AT6558

BDS/GNSS Full Constellation SOC Chip

Data Sheet

Version：1.14

Hangzhou ZhongKe Microelectronics CO.,Ltd	Title	AT6558 BDS/GNSS Full Constellation SOC Chip
	Type	Data sheet
	Number	
Document summary		
This manual provides the functional characteristics of the AT6558, the chip overview and introduction.		

Directory

1 Summary

1.1 Chip Introduction

AT6558 is a high-performance BDS/GNSS multi-mode satellite navigation receiver SOC single chip, on that integrated RF front-end, digital baseband processor, 32 bit CPU RISC, power management functions.

AT6558 support a variety of satellite navigation systems, including the Chinese BDS (Beidou satellite navigation system), American GPS, Russian GLONASS, EU Galileo, Japanese QZSS and Satellite enhanced system SBAS (WAAS，EGNOS，GAGAN，MSAS）).AT6558 is a real sixes in one multi-mode satellite navigation and positioning chip, can simultaneously receive GNSS signals of six satellite navigation systems and implement joint positioning, navigation, and timing.

1.2 Function Combination Table

Type	Multimode Function			Power		Interface		Characteristic					
	GPS	BDS	GLONASS	2.7V~3.6V	1.65V~3.6V	UART1	UART2	Flash	TCXO	Antenna Detection	Antenna Over Current Protection	Pre-SAW	External LNA
AT6558-5N-1X	•			•		•	•	•	•	•	•	•	•
AT6558-5N-2X		•		•		•	•	•	•	•	•	•	•
AT6558-5N-3X	•	•		•		•	•	•	•	•	•	•	•
AT6558-5N-5X	•		•	•		•	•	•	•	•	•	•	•
AT6558-5N-7X	•	•	•	•		•	•	•	•	•	•	•	•

1.3 Main Features

- Functional Specifications
  - Support BDS/GPS/GLONASS satellite navigation single system positioning and multiple system joint positioning
  - Support QZSS and SBAS system
  - Support A-GNSS
  - Support D-GNSS differential positioning
  - The maximum positioning update rate can reach 10Hz
- High Performance Solutions
  - Cold start capture sensitivity: -148dBm
  - Tracking sensitivity: - 162 dBm
- Low Power
  - BDS/GPS dual mode continuous operation: <23mA (@3.3V)
  - Standby: <10uA (@3.3V)
- Power Management
  - Support 2.7~3.6V power supply, typical 3.3V power supply.
  - RTC and backup power supply can be reduced to 1.5V
  - Core voltage of 1.2V
- Serial Interface
  - 2 independent UART interface
  - one I2C interface
  - 2 independent SPI interface
- Package and Size
  - QFN package, 40 pin, chip size: 5mm×5mm×0.8mm

1.4 Performance Indicators

Technical Parameters	**Indicators**
Signal receiving	BDS/GPS/GLONASS/GALILEO/QZSS/SBAS

RF channel number	Three-channel RF, support the full constellation BDS, GPS and GLONASS receiving at the same time
Cold Start TTFF	≤32s
Hot start TTFF	≤1s
Recapture TTFF	≤1s
Cold start capture sensitivity	-148dBm
Hot start capture sensitivity	-156dBm
Recapture sensitivity	-160dBm
Tracking sensitivity	-162dBm
Positioning Precision	<2m（1σ）
Speed Measurement Precision	<0.1m/s（1σ）
Timing Precision	<30ns（1σ）
Positioning Update Rate	Maximum 10Hz

1.5 Chip Application

- Vehicle positioning and navigation
- Timing
- Wearable Devices
- Portable devices, such as Mobile phone、Tablet PC

2 Pin Description

2.1 Pin Arrangement

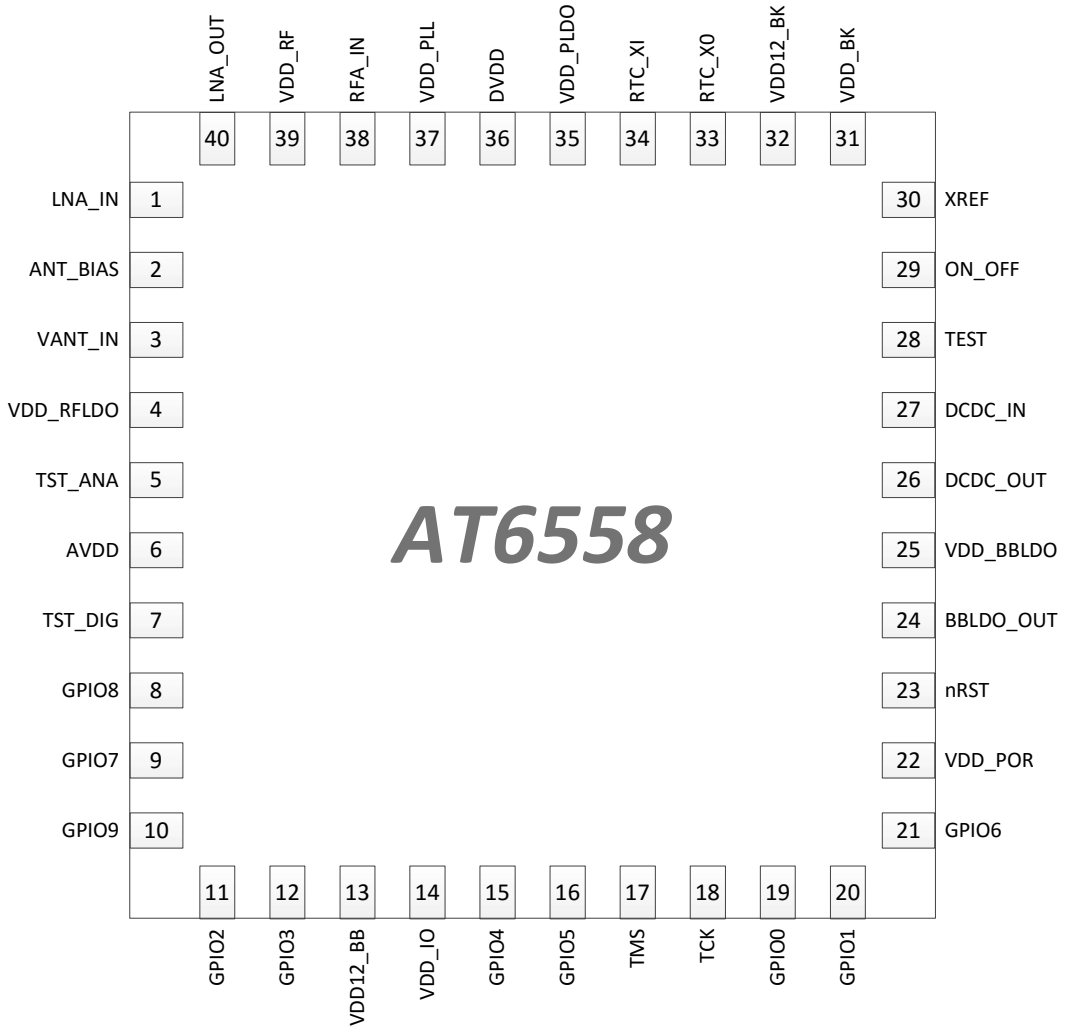


Figure 2-1 Pin arrangement for chip package

2.2 Pin Description

Number	Name	I/O Type	Function description
1	LNA_IN	Analog IO	LNA input, the internal has been separated.
2	ANT_BIAS	Analog IO	Active antenna power supply, receiving antenna

3	VANT_IN	Analog power	Active antenna power supply, max 3.6V
4	VDD_RFLDO	Analog power	RFLDO power,1.4~1.8V
5	TST_ANA	Analog IO	Analog test port
6	AVDD	Analog power	LDO output,1.2V, 1uF capacitance bypass to the ground
7	TST_DIG	Analog IO	Digital test port, the output high level is 1.2V
8	GPIO8	Digital bidirectional	General GPIO, default for speed pulse input 1
9	GPIO7	Digital bidirectional	General GPIO, default for vehicle travel direction
10	GPIO9	Digital bidirectional	General GPIO, default for speed pulse input 2
11	GPIO2	Digital bidirectional	General GPIO, default for SCL clock line of I2C
12	GPIO3	Digital bidirectional	General GPIO, default for SDA data line of I2C
13	VDD12_BB	Digital power	Digital baseband core power supply,1.2V,1uF capacitance bypass to the ground
14	VDD_IO	Digital power	Digital baseband IO power supply
15	GPIO4	Digital bidirection	Generic GPIO, default for TXD send data lines of UART1

		al	
16	GPIO5	Digital bidirectional	Generic GPIO , default for RXD receive data lines of UART1
17	TMS	Digital bidirectional	SWD debug interface data line
18	TCK	Digital input	SWD debug interface clock line
19	GPIO0	Digital bidirectional	Generic GPIO, default for TXD send data lines of UART0
20	GPIO1	Digital bidirectional	Generic GPIO, default for RXD receive data lines of UART0
21	GPIO6	Digital bidirectional	Generic GPIO, default for 1PPS output pulse
22	VDD_POR	Analog power	POR power input, battery backup main power supply
23	nRST	Analog IO	External reset input, pull-up
24	BBLDO_OUT	Analog IO	BBLDO output,1.2V
25	BBLDO_IN	Analog power	BBLDO input,1.4V~3.6V
26	DCDC_OUT	Analog IO	DCDC output
27	DCDC_IN	Analog power	DC-DC input
28	TEST	Digital	Chip test mode control, high level enter the test

		input	mode; drop down (battery backup domain)
29	ON_OFF	Digital input	Shutdown control, pull up(battery backup domain)
30	XREF	Analog IO	Reference frequency input, external TCXO or passive crystal
31	VDD_BK	Analog power	Backup power input,1.5~3.6V
32	VDD12_BK	Analog IO	Backup LDO output, 1.2V, 1uF capacitance bypass to the ground
33	RTC_XO	Analog IO	RTC OSC output
34	RTC_XI	Analog IO	RTC OSC input
35	VDD_PLDO	Analog power	PLL LDO power,1.4~1.8V
36	DVDD	Analog IO	Phase-locked loop digital power supply, 1.2 V, 1uF capacitance bypass to the ground
37	VDD_PLL	Analog IO	Phase-locked loop analog power supply, 1.2 V, 1uF capacitance bypass to the ground
38	RFA_IN	RF IO	RFA input, the internal has been separated
39	VDD_RF	Analog IO	RF power,1.2V,1uF capacitance bypass to the ground
40	LNA_OUT	RF IO	LNA output, the internal has been separated.
EP	GND	Package bottom metal	Public access sites must be well grounded.

3 Chip Architecture

3.1 Chip Block Diagram

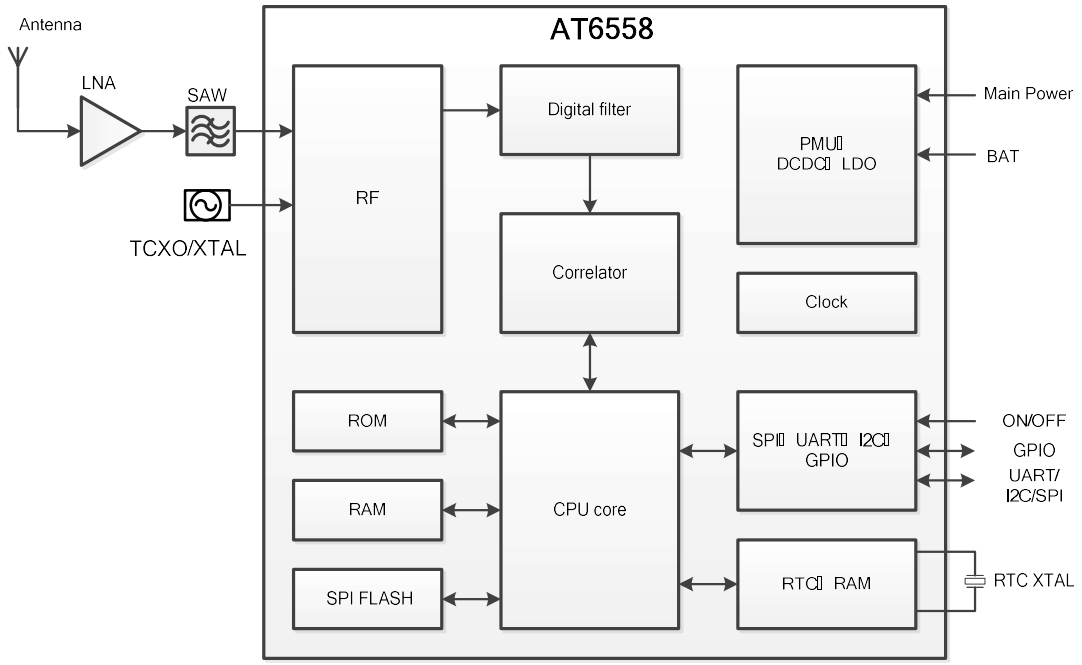


Figure 3-1 AT6558 system block diagram

3.2 Power Management

3.2.1 Low Power Supply Connection Scheme

As shown in Figure 3-2, MAIN POWER provides 3.3 V power supply to the entire chip:

Connected to VDD_IO and supplied power to IO PAD and FLASH of the chip;

Connected to VDD_POR and supplied power to internal POR , at the same time, supplied power to backup area through a diode;

Connected to the input end of the DCDC and supplied power to DCDC. Using DCDC output as an internal LDO input, supplied power to the chip RF front-end part, analog and digital part by the internal LDO.

The external button battery is used as a backup power supply (VBAT) to supply power to the backup area of the chip, and the power supply of the backup circuit can be supplied in the case of the main power supply power down.

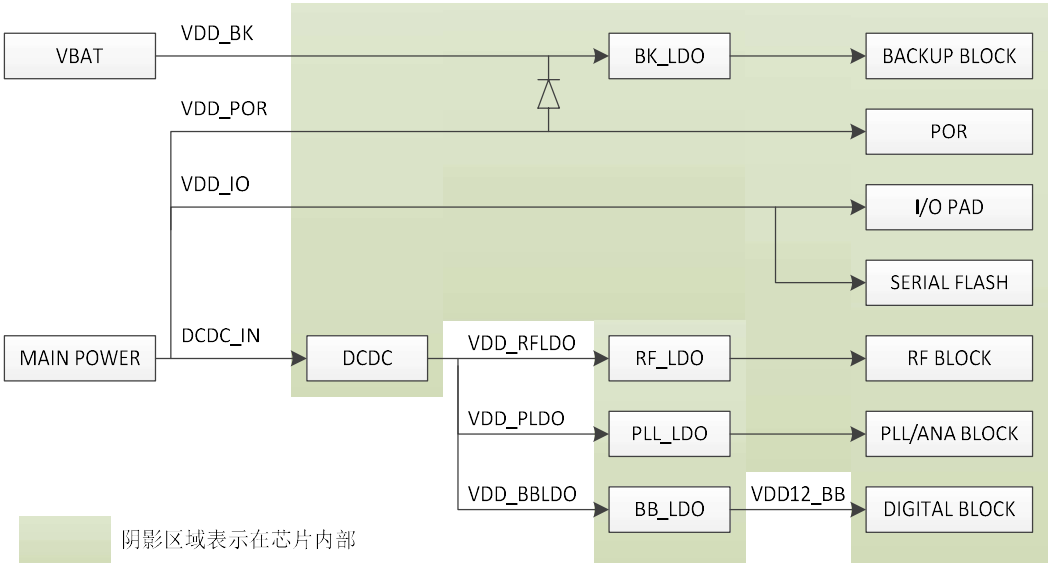


Figure 3-2 AT6558 power connection scheme (low power consumption scheme)

3.2.2 External PMU Power Connection Scheme

In the case of external PMU, DCDC and BB_LDO inside the chip can not be used, external PMU provide 3 sets of power supply for each part of the chip power

supply:

As shown in Figure 3-3, external PMU provide 3.3 V power supply ; connected to VDD_IO and supplied power to IO PAD and FLASH of the chip; connected to VDD_POR and supplied power to internal POR, at the same time, supply power to the backup area through a diode.

External PMU provide 1.5V power, connected to the RF_LDO and BB_LDO inside the chip and supplied power to RF front end and analog part of the chip by the internal LDO.

External PMU provide 1.2V power, connected to VDD12_BB inside the chip, directly to supply power to the digital part of the chip.

The external button battery is used as a backup power supply (VBAT) to supply power to the backup area of the chip, and can be supplied in the case of the main power supply power down.

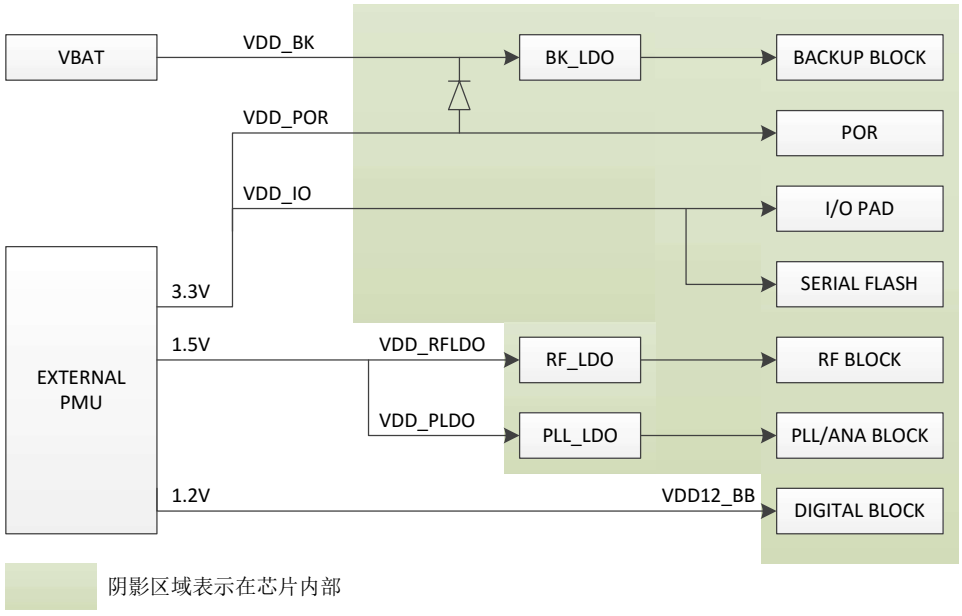


Figure 3-3 AT6558 power connection scheme (external PMU scheme)

3.2.3 Backup Power Supply

An external rechargeable 3V button battery or Fala capacitor is recommended to provide backup power for RTC and RAM. The built-in trickle charging circuit and

reverse charging circuit and don't need external diode and a current limiting resistor. The maximum charge current is 500uA and the maximum charge voltage is VDD_POR. Note that the maximum charging voltage of the button cell can reach VDD_POR-0.3V; if the Fala capacitor is used, the withstand voltage of the capacitor should be paid attention to.

If the system does not require hot start function, the VDD_BK pin can be left floating. When the VDD_POR power down, RTC and backup RAM because there is no power supply, will stop working. Positioning information can not be saved and the hot start function will fail.

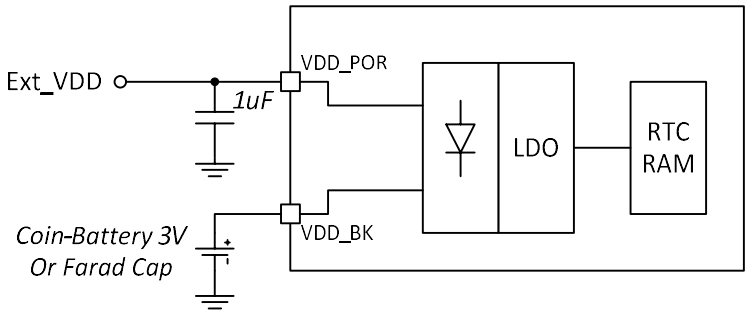


Figure 3-4 backup power connection diagram

3.2.4 Working Mode

AT6558 has four work modes: full working mode, automatic low power mode, external control low power mode and the battery backup mode.

Full working mode: when all power supply normally and the ON_OFF pin is high, the chip is in full working mode and the signal receive and calculating normally.

Automatic low power mode: in some applications, it does not need continuous positioning and more focus on low power consumption, at this time the need for timely closure of the chip function in order to save power consumption. In this mode, all the power supply normally, once the chip is working properly and positioning, the internal program will automatically shut down the power consumption module, enter the state of low power consumption and start the timer (RTC timer). The timer will automatically wake up the chip and carry on the next position.

External control low power mode: all the power supply normally and the chip is working properly, the external host will pull down the ON_OFF pin; Program inside

the chip will automatically save the current state of the circuit, and close the RF circuit and baseband circuit, then enter the state of low power consumption. When the ON_OFF pin is pulled up, the chip will automatically restore the full working mode (equivalent to a hot start).

Battery backup mode: close all the power except VDD_BK, the chip will enter the backup mode. At this time, only the minimum current is required to maintain the RTC clock and backup RAM .After the power recovery, the navigation program can recover from the backup RAM in order to achieve a rapid hot start.

Mode	RF Front-end	Baseband kernel	IO/POR	RTC/ Backup RAM
Full working mode	√	√	√	√
Automatic low power mode	×	×	√	√
External control low power mode	×	×	√	√
Battery backup mode	×	×	×	√

3.3 Chip Reset

Chip internal integrated power on reset circuit, and supports external reset from the chip. Reset sequence is as follows:

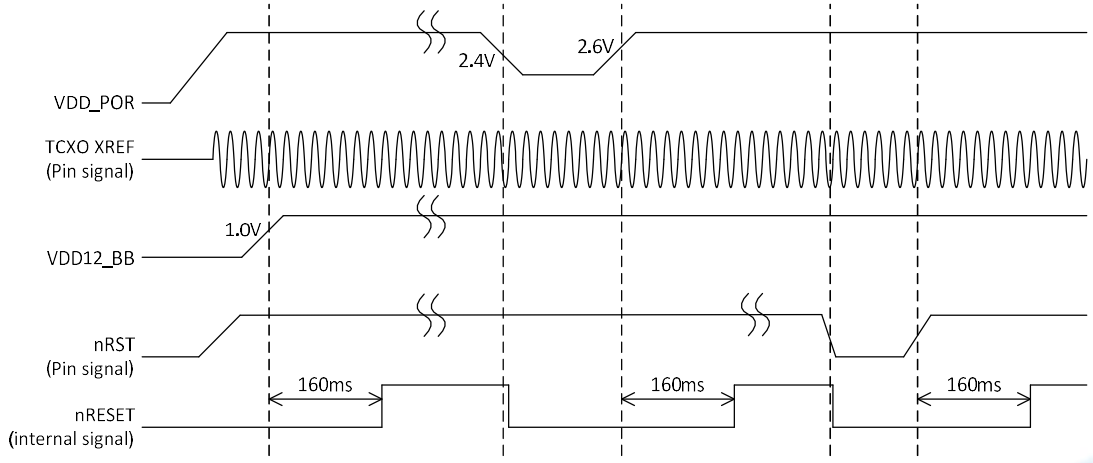


Figure 3-5 Sequence diagram of the chip reset

4 RF Front-End

4.1 RF Front-end Architecture

The RF front-end includes three separate receiving channels ,and supports the satellite signal frequency point of the full constellation: BDS B1、GPS L1、Galileo L1、GLONASS L1. Three channels sharing RF front end and PLL, support a variety of reference frequency. Integrated active antenna detection circuit and clock frequency multiplier circuit.ADC sampling frequency can be configured.

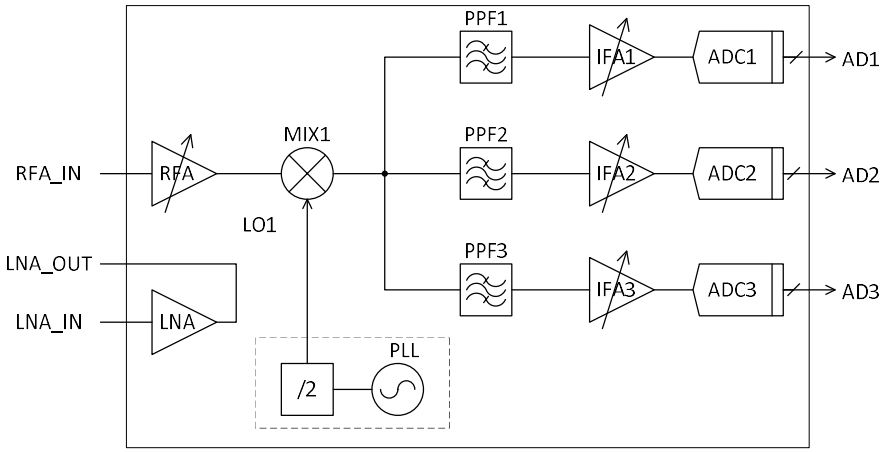


Figure 4-1 AT6558 block diagram of RF front end

4.2 Active Antenna Detection

Chip integrated active antenna detection circuit, can be fed to the external active antenna. And according to the size of the feed current, indicating the status of the active antenna. The active antenna detection circuit also provides short circuit protection, and protecting the chip and the active antenna is not damaged by limiting the current fed to the active antenna.

Detection circuit of the active antenna defines three kinds of state, when the current is less than the set value, indicating open antenna; when the current is greater than the set value, indicating a normal antenna; when the current is too large or the short circuit occurs, indicating antenna over current.

5 Baseband Processor

5.1 Multi System Satellite Processing Engine

AT6558 integrates the latest multi-system satellite processing engine, supports BDS, GPS, GLONASS, Galileo, QZSS and SBAS system. It can receive the signals of the six systems at the same time and realize the joint positioning. AT6558 can significantly improve the positioning accuracy and positioning availability, especially in the complex environment, such as urban canyons, performance improvement is more significant.

5.2 RTC Backup Area

Real time clock (RTC) is located in the battery power supply area, and is equipped with a backup RAM. Using independent low power LDO for power supply. RTC can normally work in the case of the disappearance of the main power supply, while ensuring that the data is not lost in the backup RAM.

5.3 Timer

Using three timer circuit with PWM function, the timer interrupt can be used as a processor interrupt input, also can be used as the hardware request source of DMA. The timing cycle can be adjusted according to re-frequency-dividing of the peripheral clock, theoretically up to 2^{32} times of the peripheral cycle.

5.4 DMA Controller

DMA controller supports one-way transmission of 8 channels, each channel can be independently carried out the following three kinds of data transmission: memory to the peripheral; peripheral to the memory; memory to the memory.

5.5 Watchdog

Watchdog circuit is used for the detection of hardware and software, whether a timeout error has occurred. When there is a timeout signal output, the chip will be reset by the signal. Therefore, the reliability of the chip is guaranteed from the

hardware.

5.6 UART

Consists of two independent full duplex UART modules, achieve data conversion between serial and parallel. Baud rate maximum support 256000bps, and have the function of automatic baud rate detection. Each UART has an independent transmit FIFO and receive FIFO, the depth is 32 bytes. UART supports DMA working mode.

5.7 SPI

AT6558 contains a SPI master device interface and a SPI slave device interface. SPI master device interface is used for connecting the SPI interface devices, such as MEMS sensors, FLASH, etc.. SPI slave the device interface can be used as the data interface with the external application processor, the external application processor through the SPI interface to obtain the location information of the chip. Compared to UART, the data transmission speed of SPI is significantly improved.

5.8 I2C

I2C interface as the master device interface can carry standard transmission (100Kbps) and fast transmission (400Kbps). Support 7bit address or 10bit address mode. Both receiving and sending contain 4 bytes FIFO depth, can be configured for DMA working mode .

6 Electrical Characteristics

6.1 Limit Characteristics

Parameters	Maximum swing	Unit
Voltage referring to earth(analog core power supply, digital core power supply)	-0.3 ~ 1.8	V
Voltage referring to earth(digital IO rear drive power supply, LDO input power supply)	-0.3 ~ 4.1	V
Analog pin voltage	-0.3 ~ 1.8	V
Other pin voltage	-0.3 ~ 4.1	V
Maximum RF input power	5	dBm
Working Temperature	-40~85	℃
Junction Temperature	150	℃
Storage Temperature	-50~125	℃

6.2 DC Characteristics

Power Pin

Parameters	Minimum value	Typical value	Maximum value	Unit
VDD12_BB	1.08	1.2	1.32	V
VDD12_BK	1.08	1.2	1.32	V
VDD_IO	2.7	3.3	3.6	V
VDD_POR	2.7	3.3	3.6	V
VANT_IN	1.8	3.3	3.6	V
VDD_BK	1.5	3.3	3.6	V
VDD_PLDO	1.4	1.5	1.8	V
VDD_RFLDO	1.4	1.5	1.8	V
VDD_BBLDO	1.4	1.5	1.8	V
DCDC_IN	2.7	3.3	3.6	V
DCDC_OUT	1.4	1.5	1.75	V
AVDD	1.14	1.2	1.26	V
DVDD	1.14	1.2	1.26	V
VDD_RF	1.14	1.2	1.26	V
VDD_PLL	1.14	1.2	1.26	V
BBLDO_OUT	1.14	1.2	1.26	V

Digital IO Pin

Parameters	Instruction	Minimum value	Typical value	Maximum value	Unit
Ileak	Leak current input pin	---	<1	---	uA
Vil	Low level input voltage	-0.3	0	VDD_IO*0.2	V
Vih	High level input voltage	VDD_IO*0.8	---	VDD_IO+0.3	V
Vol	Low level output voltage	---	0	0.4	V
Voh	High level output voltage	VDD_IO-0.4	---		V
Rpu	Pull up resistor		40		kΩ
Rpd	Pull down resistor		40		kΩ

6.3 Simulation Related Characteristics

NO.	Parameters	Condition	Parameter Index			Unit
			Minimum value	Typical value	Maximum value	
1	Reset voltage		2.35	2.45	2.6	V
2	Reset time [1]	crystal frequency 26.000MHz		160		ms
3	TCXO crystal frequency [2]			26.000		MHz
4	TCXO amplitude		0.5	1.5	3.6	Vpp
5	Crystal frequency [2]		10	26.000	32	MHz
6	Crystal equivalent series resistance *Rs*				80	Ω
7	Active antenna detection current [3]		2.4	3	3.6	mA
8	Active antenna short-circuit protection current [4]		45	50	60	mA
9	Antenna detection circuit voltage drop	Input 50mA, 3.3V load			0.3	V
10	Working current	@3.3V BD+GPS		23		mA
11	Battery backup current			10	40	uA

12	RTC Crystal frequency			32.768		kHz
13	RTC Crystal equivalent series resistance *Rs*				80	KΩ

[1] Reset time is related to the crystal frequency. When the frequency is 16.369MHz, the reset time is 250mS, and the frequency is 26 MHz, the reset time is 160 mS.

[2] Chip use the 26.000MHz frequency TCXO by default. Other frequencies as well as passive crystal need to customize the program.

[3][4]Active antenna detection current and short circuit protection current can be configured.

6.4 RF Related Characteristics

NO.	Parameters	Condition	Parameter Index			Unit
			Minimum value	Typical value	Maximum value	
1	Input frequency F_{in}	GPS		1575.42		MHz
		Galileo		1575.42		MHz
		BD		1561.098		MHz
		GLONASS	1597.78	1602	1605.66	MHz
2	Input signal level P_{IN}		-110		-65	dBm
3	Input reflection coefficient S11				-10	dB
4	Noise figure NF			2.5		dB
5	1dB compression point			-75		dBm
6	Image rejection ratio		16	26		dB
7	Lock time of phase locked loop				100	us
8	AGC stable time				100	us

6.5 Satellite System Model

Chip provides a combination of multiple satellite system model, as follows. Considering the bandwidth, group delay and RF port matching, etc., please choose the

appropriate SAW filter and antenna..

Model	GPS	BD	GLONASS
1	●		
2		●	
3			●
4	●	●	
5	●		●
6		●	●
7	●	●	●

7 Interface Properties

7.1 RS232 Interface Timing

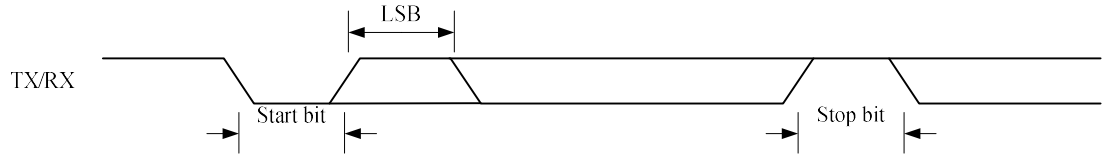


Figure 7-1 RS-232 interface timing diagram

7.2 SPI Interface Timing

Description	Label	Minimum	Maximum	Unit
CS establishment time	T1	0.5T	-	ns
CS hold time	T2	0.5T	-	ns
SDO establishment time	T3	0.5T - 3t	0.5T - 2t	ns
SDO hold time	T4	0.5T + 2t	0.5T + 3t	ns
SDI establishment time	T5	3t	-	ns
SDI hold time	T6	10	-	ns

Note1:T represents SCK time cycle, configurable range is （SPICLK/2）MHz ~ （SPICLK/4096）MHz.

Note2: t represents SPICLK time cycle, can be a high-speed bus clock or peripheral clock.

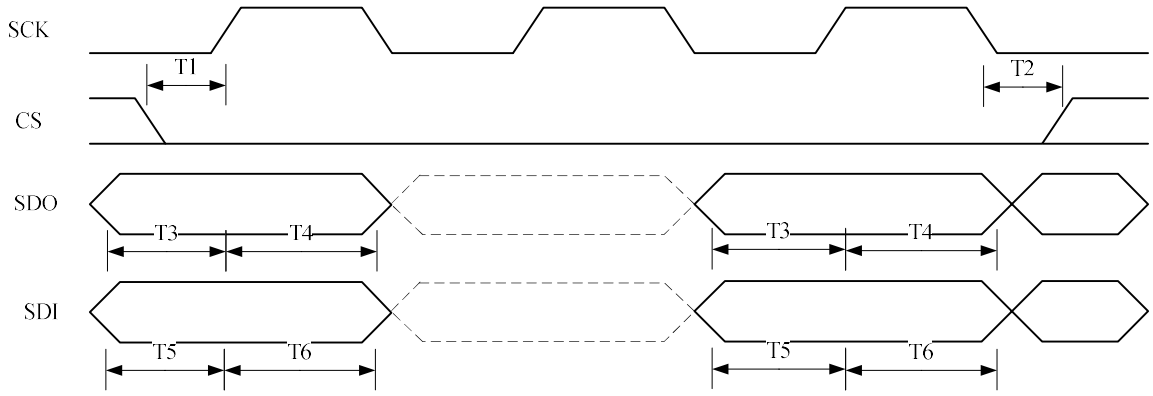


Figure 7-2 SPI interface timing diagram

7.3 SWD Interface Timing

Description	Label	Minimum	Maximum	Unit
The establishment time of the TMS (I) input to the TCK rising edge	T1	0.35T	-	ns
The hold time of the TMS (I) input to the TCK rising edge	T2	0.15T	-	ns
The data valid time of the TCK rising edge to TMS (O) data	T3	-	0.5T	ns
The hold time of the TCK rising edge to TMS (O)	T4	0	-	ns

Note: T represents the cycle of the JTAG interface TCK, the maximum is 50MHz.

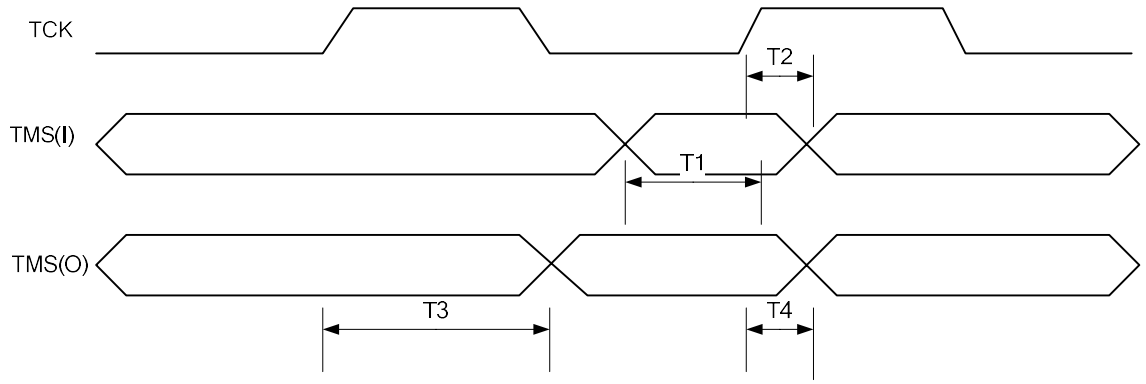


Figure 7-3 SWD interface timing diagram

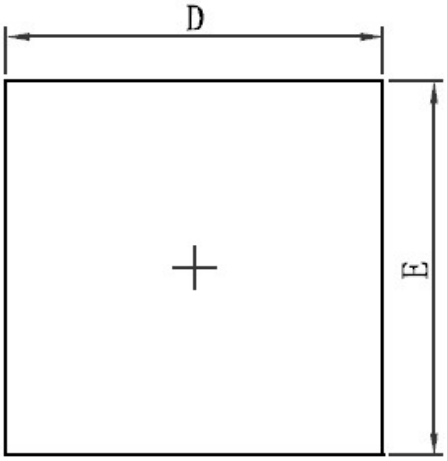
8 Chip Package

8.1 Chip Identification Rules

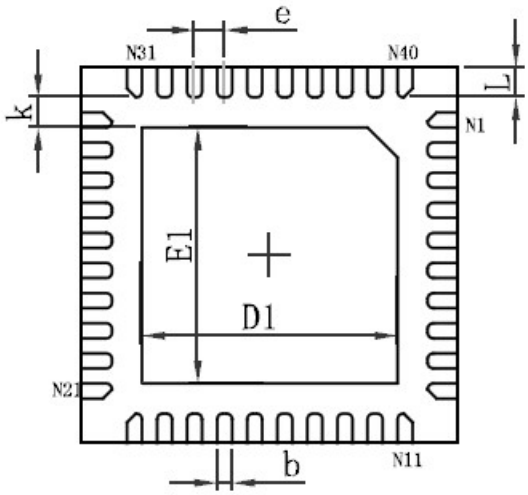
Code	Instruction
AT6558	Chip model
LLLLLLLLLLL	Chip serial number

8.2 Package Specification

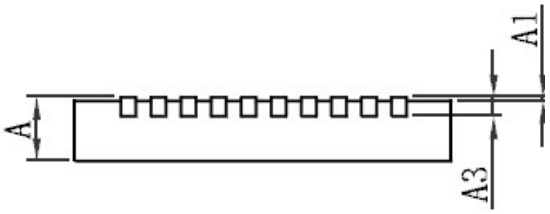
The chip is packaged in the form of QFN5 * 5-40L (P0.4T0.8) , the following is the size of the package.



Top View



Bottom View



Side View

Package Size

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.324	0.476	0.013	0.019

9 Reference Design

9.1 Reference Scheme

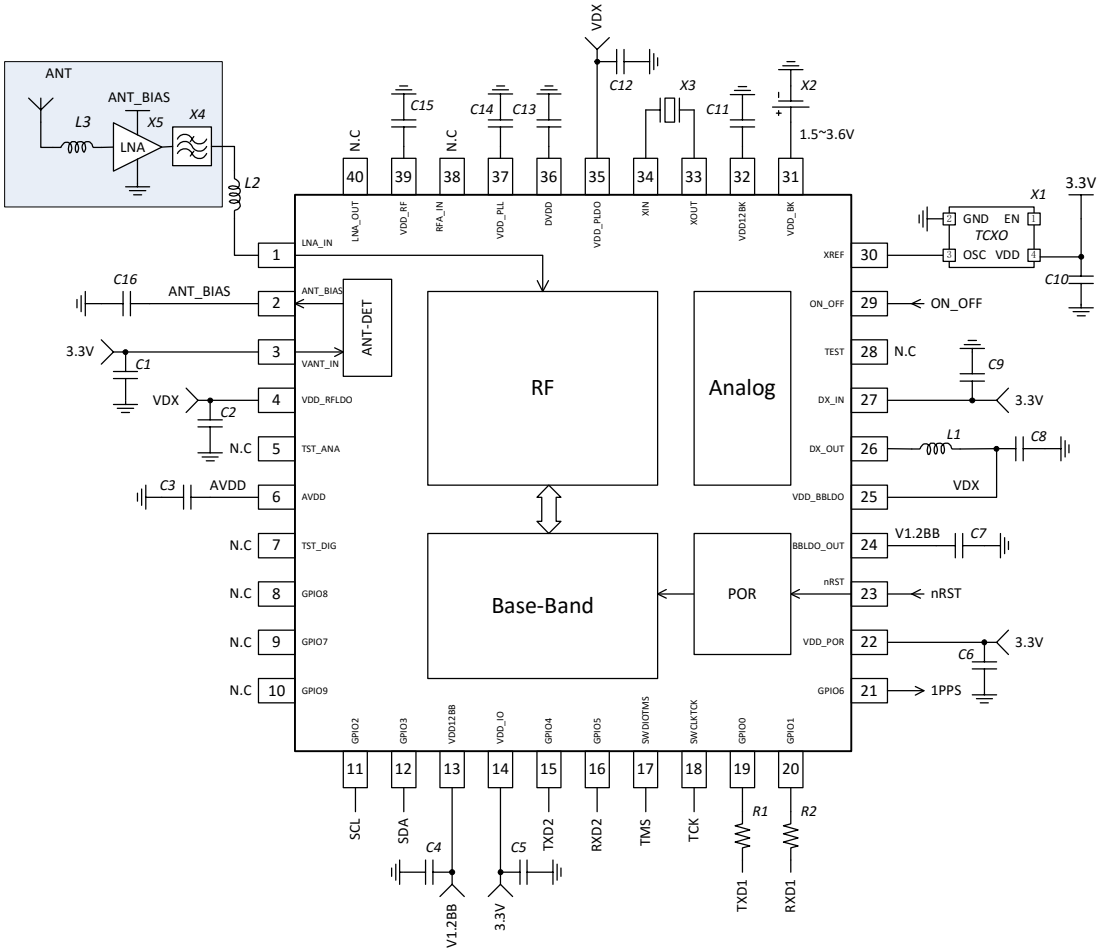


Figure 9-2 passive antenna scheme

The scheme adopts the passive or active antenna, the total gain outside the chip is more than 18dB, less than 35dB. The LNA of an active antenna or a passive antenna is powered by ANT_BIAS. Note that LNA_IN DC voltage is less than 1.2 V. If the antenna unit circuit output is DC, before the inductor L2 must add a 470pF blocking capacitor. Positioning information through the serial port output, the default output port is the UART1, corresponding to TXD1/RXD1. Material list: device selection please refer to "AT6558 main peripheral components BOM table"

Number	Optional

C1、C2、C4、C5、C6、C9、C10、C12、C17	0.1uF±5% Chip capacitor
C3、C7、C11、C13、C14、C16	1uF±5% Chip capacitor
C8	10uF±5% Chip capacitor
C15	470pF±5% Chip capacitor，Used as a DC-block
R1、R2	10k Ohm±5% Chip resistor
L1	4.7uH±10% Chip inductor
L2	4.3 nH±5% High frequency chip inductor
L3	5% High frequency chip inductor According to the LNA input impedance matching fixed value
X1	TCXO Crystals，Recommend 0.5ppm
X2	3V rechargeable button battery or super capacitor
X3	RTC Crystals，32.768kHz
X4	SAW Filter
X5	External LNA

9.2 Device Selection

AT6558 main peripheral components BOM table

Device name	Parameters	Package	Specifications	Manufactor	Model
DC/DC Power Inductors	4.7uH	0603	±20%,620mA,0.5Ω	SAMSUNG	CIG10W4R7MNC
				MURATA	LQM18PN4R7MFR
High Frequency Inductors	4.3nH	0402	±0.2nH,750mA,0.07Ω	MURATA	LQW15AN4N3C00D
			±0.3nH,300mA,0.21Ω		LQG15HN4N3S02
	6.8nH		±3%,570mA,0.13Ω		LQW15AN6N8H00D
			±5%,300mA,0.29Ω		LQG15HN6N8J02
	33nH		±3%,260mA,0.63Ω		LQW15AN33NH00D
			±5%,200mA,0.67Ω		LQG15HN33NJ02
RTC Crystals	32.768K	SMD3215	20ppm,CL=12.5pF	EPSON	FC-135
				KDS	DST310S
TCXO Crystals	26M	SMD2520	3.3V, 0.5ppm@-30℃to +85℃ or 0.5ppm@-40℃to +85℃	EPSON	TG-5035CG
					TG-5006CG
				KDS	DSB221SDN
				KYOCERA	KT2520K26000ACW33T
				NDK	NT2520SB
				TXC	7L26003
				SIWARD	STO-2520A
Low Noise Amplifier	LNA	6UDFN	Gain=21.5dB,NF=0.8dB	Hangzhou Zhongke	AT2659

				Micro	
Filter	SAW	SMD1411	Insertion Loss= 0.9dB@1575.42M impedance=50Ω	TDK EPCOS	B39162B9416K610
			Insertion Loss = 0.95dB@1575.42M impedance=50Ω	MURATA	SAFEB1G57KE0F00
			Insertion Loss = 0.9dB@1575.42M 1.3dB@1602M, impedance=50Ω		SAFEA1G58KA0F00
			Insertion Loss = 1.0dB@1575.42M 1.3dB@1602M, impedance=50Ω	WISOL	SFHG89DQ102

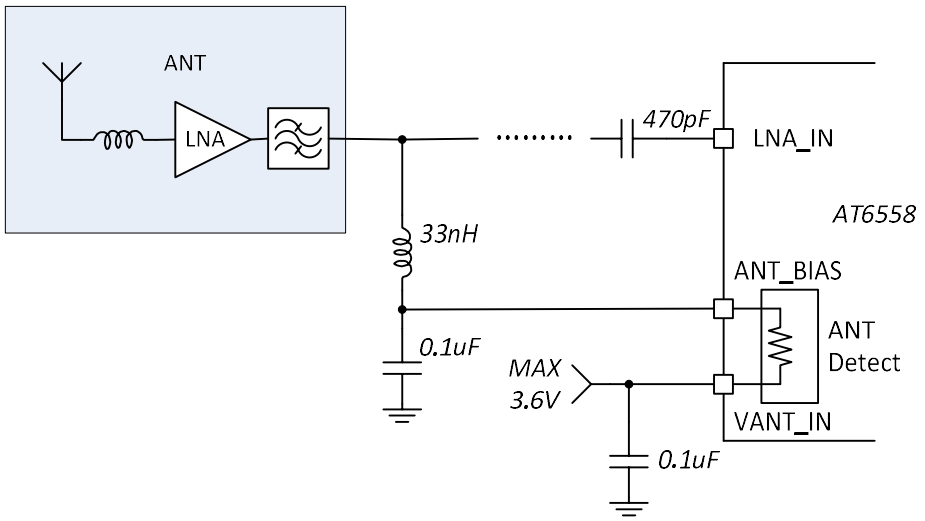
10 Application Solutions

10.1 Active Antenna Feed and Detection

The following figure, the chip active antenna detection circuit can detect the state of the active antenna, VANT_IN connected to a system power supply, the maximum voltage 3.6V.ANT_BIAS connected to a 33nH and 0.1uF inductor capacitor filter for blocking the AC signal, and feed to the active antenna.

Note: Even if the LC filter is added to block AC signal, low frequency communication large signal is still likely to feed through to ANT_BIAS port and cause detection circuit miscalculation. Especially in the strong interference environment or near the high power transmission device, the probability of miscalculation will increase.

The minimum detection current for antenna access is 2.5mA, and the current limit of short circuit protection is 50mA.



10.2 RF Input

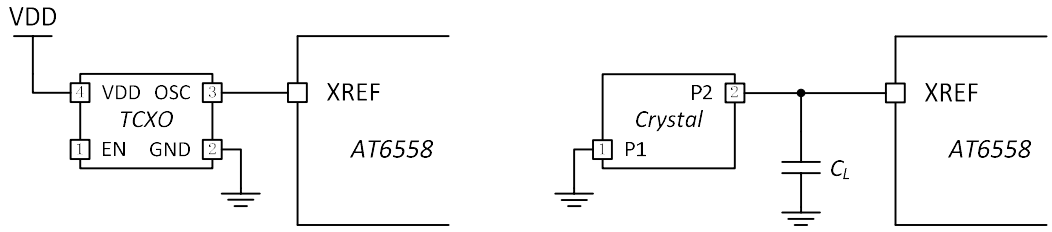
Signal input from the LNA_IN, external antenna unit (passive medium +LNA, or active antenna) is recommended for the gain of 18~35dB. No matter what form of the antenna, it is recommended to carry out the power supply through the ANT_BIAS. The chip can automatically adjust the internal gain by the state of the antenna, so that the chip can work in the optimum gain state.

10.3 Reference Clock Oscillator

The reference clock frequency stability will greatly affect the receiver performance, including sensitivity, positioning accuracy, timing accuracy. Normally, in order to obtain the optimal performance, it is recommended that the user chooses high stability crystal oscillator for clock reference source of navigation chip. Recommended temperature compensated crystal oscillator which frequency stability is 0.5ppm, and is not sensitive to temperature and vibration environment.

The chip also supports passive crystal as a clock reference source, due to passive crystal instantaneous frequency drift is large, positioning accuracy is inferior to TCXO. Due to the passive oscillator frequency is not fixed and the precision is poor, every batch of navigation firmware of passive crystals need to customize, so don't recommend to use passive crystals.

Commonly used the circuit connection of active crystals and passive crystals are as follows:



Active crystals Passive crystals

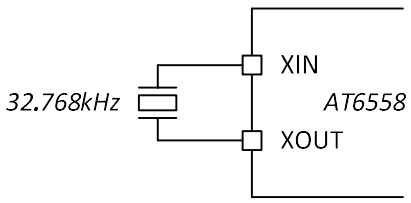
(Chip firmware needs to be customized)

P1 which is one end of the passive crystal connect to ground, and P2 which is the other end of the passive crystal connect to chip XREF, at the same time , a capacitor CL is connected in parallel to the ground on P2. The value of CL is the load capacitance of the crystal. Different crystals may be different, the general 12pF can be.

10.4 RTC Clock

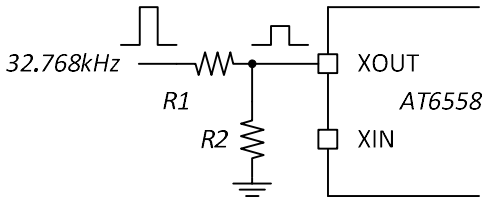
Real time clock (RTC) is located in the battery power supply area, which ensures that the Backup data in RAM is not lost when the main power supply is off .When the main power supply is power on again, it can quickly re-positioning. RTC OSC using

passive crystal, connected to the XIN and XOUT pins of the chip, without the off-chip capacitor and the feedback resistor, as shown below:



32k RTC Passive crystal

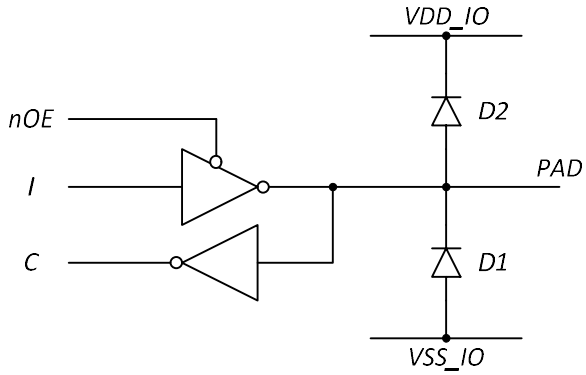
Chip also supports the direct clock input, the user can choose from the XIN or XOUT input, but need to ensure that the instantaneous voltage on the XIN or XOUT not more than 1.5 V.As shown below, the clock signal is added to the XOUT through the resistor voltage divider, and adjust the ratio of R1 to R2, so that the clock high level on the XOUT is 1.2V.



32K direct clock input (resistor voltage divider)

10.5 GPIO

Chip provides 10 GPIO, can be reused for UART, I2C, SPI, etc.. Its main internal structure is as follows:



It must keep the PAD voltage which is less than VDD_IO+0.5V in use, otherwise it will appear ESD diode D2 forward conduction and lead to the chip working abnormal.

Special note: when the GPIO as the input IO, such as RXD1/RXD2, chip

VDD_IO power down, the external device should set the GPIO port signal voltage to low level.

10.6 Low Power Setting

AT6558 can provide two kinds of low power solution those are automatic low power mode and external control low power mode.

Automatic low power consumption mode is that in the non continuous positioning scenarios, the chip positioning, internal procedures automatically turn off the power module, enter standby mode; Wake up automatically and carry on the next position by the timer. According to the different application scenarios, the program needs to customize.

External control low power mode has three kinds of way1) shut down the main power supply; 2) set ON_OFF pin to low level; 3) send low power instructions through the UART.

Power mode		Core	IO/POR	LNA	TCXO	Antenna	RTC	Main power supply
Full working mode		√	√	√	√	√	√	ON
Automatic low power mode		×	√	×	×	×	√	ON
External control low power mode	Shut down main power supply	×	×	×	×	×	√	OFF
	ON_OFF Pull down	×	√	×	×	×	√	ON
	UART instructions	×	√	×	√	×	√	ON

10.6.1 Enter Low Power Mode

1）Shut down main power supply

In the power connection as shown in the figure below, shut down the main power supply VMAIN. In addition to the backup circuit, all other circuit power down, power consumption is close to 0.

Special note: the GPIO as input, such as RXD1 / RXD2, chip VDD_IO power down, the external device should be set the signal voltage of the GPIO port to low level.

2）Set the ON_OFF pin to a low level

Mains VMAIN electricity normally, ON_OFF pin is set to the low level through external MCU, the chip will enter a low-power standby state, the chip consumes only minimal power consumption. External active antenna, LNA, TCXO and so on will be closed.

3）Send instruction via UART

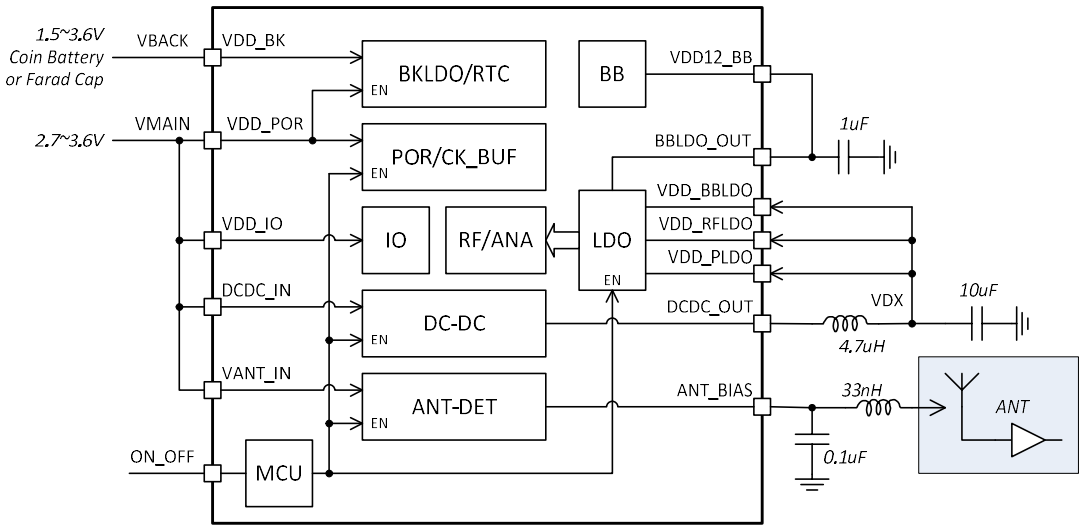
Mains VMAIN electricity normally, through external UART send instructions that enter the low power mode, the chip will shut down most of the circuit, enter the low power standby state. External active antenna, LNA and so on shut down. TCXO work normally.

4）Automatic Low Power Mode

In the sleep and wake time interval of system definition, the chip automatically enter the low power mode.

10.6.2 Peripheral Circuit Connection Solutions

1）Chip Power Supply



2) Antenna or external LNA enable

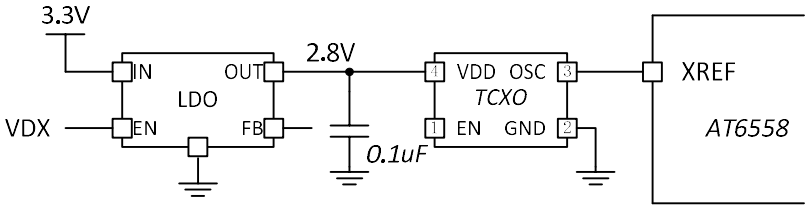
An external LNA or antenna unit is powered by ANT_BIAS and achieve enable

Normal work, the ANT_BIAS output supply power to external LNA or antenna unit; low power consumption, ANT_BIAS off, then the external LNA or antenna is closed, no longer consumes the charge current.

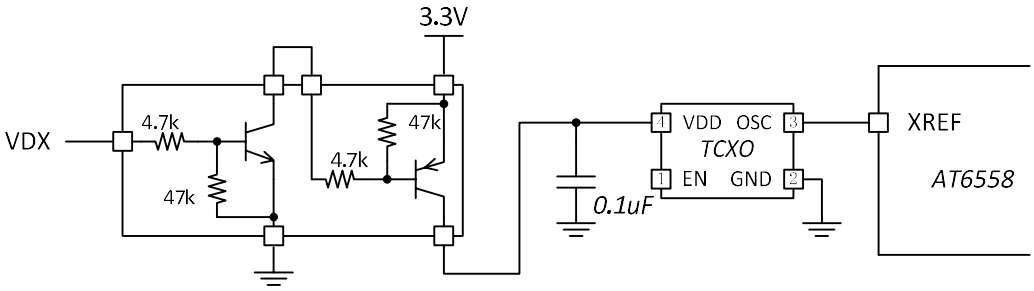
3) TCXO Power Supply

ON_OFF low power mode and independent low power mode need to close the TCXO to further reduce power consumption.

Separate LDO or NPN-PNP composite transistor chip supply power to TCXO, using the output of the chip DCDC VDX as enabling signal.



Using LDO supply power to TCXO



Using a compound transistor chip supply power to TCXO

10.7 DCDC

In order to obtain the lowest power consumption and optimal performance, it is recommended to use on-chip DCDC converter, the output of the DCDC supply on-chip LDO again. It can effectively reduce the power consumption of the chip.

In order to reduce the influence of DCDC switching frequency on the performance of the chip, the connection length of the 4.7uH inductor and the 10uF capacitor with the pin DX_OUT must be minimized. Filter circuit is particularly important, and it is recommended that each power input is added to the 1uF filter capacitor, if necessary, plus other filter power circuit.

Special attention, both ground wire that a filter capacitor of the power input DX_IN and ground wire that the filter capacitor after output DX_OUT inductance should have good connection with GND. If the ground wire is through the PCB via hole connected to the GND, should be respectively through via hole connected to the GND, and try to increase the number of via hole.

11 Packaging and Transportation

11.1 Packaging

AT6558 chip use moisture roll tape for packaging.

11.2 ESD Protection

Please pay attention to the antistatic and moisture proof in the process of chip transportation and production.

 **CAUTION!** ESD SENSITIVE DEVICE!

Please pay attention to the electrostatic protection in the process of using, packaging and transportation!

12 Document Update Record

Date	Version	Instruction
2015.06.30	V1.08	The first version of the official release
2015.07.20	V1.09	1 Modify the ANT_BIAS pin definition 2 Add backup power note 3.2.3 3 Add the power consumption mode 3.2.4 4 Add chip reset instructions 3.3 5 Modify the reference design 6 Add application solutions and recommendations section
2015.07.20	V1.10	Not supported passive crystal
2015.08.12	V1.11	1 Modify the default support for crystal frequency 2 Add a reference clock crystal selection section 10.3
2015.12.01	V1.12	1 Modify IO/POR power range to 2.8~3.6V 2 Add DCDC instructions 3 Modify passive antenna solution

		4 Add RTC clock direct input instructions 5 Add GPIO instructions 6.Add function combination instructions, including single GPS positioning, single BDS positioning, GPS+BDS dual mode positioning, GPS+GLONASS dual mode positioning, GPS+BDS+GLONASS three mode positioning 7.Update reference design in chapter 9 8.Update application solutions proposal in chapter 10 9.Other text improvement
2016.3.25	V1.13	1. Merger 9.1 active antenna solution, 9.2 passive antenna scheme is the new 9.1 reference scheme, and modify the circuit diagram 2. Revision device selection 9.2.
2016.4.7	V1.14	1 Modify scheme diagram 9.1, content 9.3 2 Modify content 10.1-10.7

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